

Application No. 09/896,780  
Response filed July 22, 2004  
Reply to Office Action dated April 22, 2004

Attorney Docket No. 032674-140  
Page 2 of 5

### REMARKS

Claims 1-35 are pending, with claims 1, 17, and 34 being in independent form.

In the Office Action, claims 1-35 have been rejected for anticipation by U.S. Patent No. 6,412,081 to Koscal et al. ("Koscal"). The Applicant believes the pending claims are allowable over the cited document for the following reasons.

Anticipation requires that every feature of the claimed invention be shown in a single prior document. *In re Paulsen*, 30 F.3d 1475 (Fed. Cir. 1994); *In re Robertson*, 169 F.3d 743 (Fed. Cir. 1999). The pending claims positively recite features that are not described in the cited document.

For example, claim 1, recites, among other things, "storing correction code in at least one of a plurality of correction blocks included in an electrically erasable programmable memory" and "executing a program having instructions stored in the memory" (emphasis added). Since only art rejections are raised in the Action, the Office has determined that the pending claims satisfy the requirement of definiteness in 37 C.F.R. § 112. Accordingly, the instructions stored in the memory (emphasized above) for executing the program are stored the same electrically erasable programmable memory that includes the correction code stored in at least one of the plurality of correction blocks included in the memory.

In contrast, Koscal describes an arrangement in which program code including a programming error is stored in a first memory, and patch code for correcting the error is stored in at least one of separate second and third memories. Koscal further describes that the program being corrected is typically stored in read-only memory (ROM) and that the patch code is typically stored in non-volatile random-access memory (NVRAM) or electrically-erasable programmable ROM (EEPROM). See col. 19-32. Nowhere does Koscal disclose that the program to be corrected and the patch code are stored in the same memory, much less the same electrically erasable programmable memory, as claim 1 requires. Accordingly claim 1 is believed to be allowable for at least this reason.

In addition, claim 1 recites storing the correction code in at least one of a plurality of correction blocks. As described by the Applicant, each of the plurality of correction blocks allocated in the flash memory is configured to store a respective portion of correction code to be patched into the main program. The respective

Application No. 09/896,780  
Response filed July 22, 2004  
Reply to Office Action dated April 22, 2004

Attorney Docket No. 032674-140  
Page 3 of 5

portions of correction code can be used to correct several different program errors in the same program or different programs being executed from the erasable programmable memory. As described by the Applicant, a corresponding number of entries in an address match interrupt register can be set up to trigger the execution of the respective portions of correction code stored in the correction blocks. See, e.g. paragraphs [0013], [0037], and [0046].

In contrast, Koscal's arrangement is capable of storing and executing patch code for correcting a single error or at best a number of errors in a contiguous segment of the program being corrected. For example, Koscal describes that:

If patch code is present, pursuant to the process, the trap address is downloaded into a holding circuit, the patch address is downloaded into a predetermined patch address vector, the patch code is optionally copied into the third memory, and an enable circuit is activated to enable the trap and patch function. A compare circuit compares addresses sent out over the address bus by the microprocessor with the contents of the holding circuit. Col. 2, l. 65 - col. 3, l. 5.

According to this portion of Koscal, patch code for only one patch is stored in the second (and possibly third memory), and only one trap address is stored in the holding circuit for comparison with the program addresses sent over the address bus. Thus, Koscal does not disclose a plurality of correction blocks as recited in claim 1, and the claim is considered allowable over the cited document for this reason as well.

Regarding claim 4, Koscal does not describe "determining for each of the correction blocks whether correction code stored in the blocks is to be executed during the executing of the program" by "retrieving a first data value from each of the correction blocks having stored correction code". The Office asserts that Koscal describes these features in column 4, lines 5-16. But this portion of Koscal merely describes an arrangement in which the current program address is compared with the patch trap address to determine if the patch should be executed. The cited portion does not describe the recited retrieving of a first data value from each of the correction blocks having stored correction code (e.g., Koscal's patch code). Accordingly, claim 4 is considered allowable for this reason as well.

Regarding claims 6-10, Koscal does not describe any of the recited "retrieving a second data value from each of the correction blocks having stored correction code", "comparing the retrieved second data value from each of the correction blocks

Application No. 09/896,780  
Response filed July 22, 2004  
Reply to Office Action dated April 22, 2004

Attorney Docket No. 032674-140  
Page 4 of 5

having stored correction code to a post address match value of the program counter", and "identifying the correction block corresponding to the invoking of the address match routine as the correction block having the second data value equal to the post address match value of the program counter". The Office asserts that Koscal describes these features in conjunction with FIG. 5, but the Applicant respectfully disagrees.

Nothing in FIG. 5 of Koscal describes retrieving a second data value from each of the correction blocks and then comparing this retrieved value with a post address match value of the program counter, e.g., a value after the correction code stored in one the correction blocks has been executed. Once the comparison is made, a determination can be made whether the appropriate correction code as been properly executed. If the code has not been properly executed, an error routine (e.g., claim 7) can be executed, or other action taken. The only blocks shown in FIG. 5 of Koscal that pertain to actions occurring after the patch code has executed are blocks 516 and 517, and these blocks do not disclose the features recited in claim 6. Accordingly, claims 6-10 are considered allowable for these reasons as well.

Regarding claims 17-33, these claims recite features that are substantially similar to claims 1-16, and are considered allowable for at the same reasons discussed above.

Regarding claims 34 and 35, claim 34 defines an electrically erasable programmable memory based memory map structure that includes, among other things, "a plurality of correction blocks for storing correction code" and "a main program area for storing at least one executable program". As discussed above, Koscal describes an arrangement in which the program containing the error and the corresponding patch code are stored in separate memories, not different areas of the same electrically erasable programmable memory as recited in claim 34. Moreover, Koscal does not describe an arrangement that includes a plurality of correction blocks. Accordingly, claims 34 and 35 are considered allowable for at least the same reasons that claim 1 is considered allowable.


Application No. 09/896,780  
Response filed July 22, 2004  
Reply to Office Action dated April 22, 2004

Attorney Docket No. 032674-140  
Page 5 of 5

For the foregoing reasons, it is believed this application is in condition for allowance and an early Notice thereof is earnestly solicited. If any questions remain, the Examiner is invited to phone the undersigned at the below-listed number.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

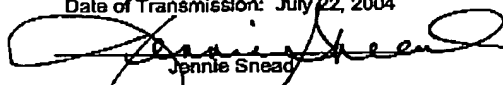
By:   
Stephen J. Tipton  
Registration No. 45,846

P.O. Box 1404  
Alexandria, Virginia 22313-1404  
(919) 941-9240

Date: July 22, 2004

I hereby certify that this correspondence is being sent by facsimile transmission to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 to the following facsimile number:

Facsimile Number: 703 872 9308  
Date of Transmission: July 22, 2004

  
Jennie Snead